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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO..	CONFIRMATION NO.
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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,523	SO ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the Applicant's submission of the amendment dated July 25, 2006. At this point, no claims have been amended, and no claims have been cancelled. There are 20 claims pending in the application; there are 4 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

2. As required by **M.P.E.P. 609(C)**, the Applicant's submissions of the Information Disclosure Statement dated July 8, 2004 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-2, 6, 12-13 and 15-19** are rejected under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948).

5. As per **claims 1, 12, 16 and 18**, Hinton discloses a method/system "of reducing the size of a translation lookaside buffer comprising utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer" as **["Translation Lookaside Buffer, TLB (11)" (Column 3, lines 23-25; Figure 1) and "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3)]**.

6. As per **claim 2 and 13**, Hinton discloses "The method of claims 1 and 12" **[See rejection to claims 1 and 12 above]** "wherein said bit corresponds to the least significant bit of said virtual page number" **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address" (Column 6, lines 37-63; Figure 3)]**.

7. As per **claim 6**, Hinton discloses "The method of claim 1" **[See rejection to claim 1 above]** "wherein said virtual address comprises 32 bits" **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62)**

are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Column 6, lines 38-43)].

8. As per **claims 15, 17 and 19**, Hinton discloses the method/system of claims 12, 16 and 18 **[See rejection to claims 12, 16 above and rejection to claim 20 bellow]** wherein said consolidating even and odd page frame numbers into a single page frame number field implements a translation lookaside buffer of reduced size **[With respect to this limitation, Hinton discloses "Translation Lookaside Buffer, TLB (11)" (Column 3, lines 23-25; Figure 1) and "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67), Hinton is implementing a TLB of reduced size as compared with Applicant's described prior art (Background of Applicant's Specification)]**.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claim 3, 5, 10, 14 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948).

11. As per **claims 3, 5, 10, 14 and 20**, Hinton discloses the method/system of claims 1, 12 and 19 **[(See rejection to claims 1, 12 and 19 above). Hinton also discloses using a translation lookaside buffer (TLB) for translating of instruction pointers from logical address to physical address (Column 3, lines 23-25) wherein instructions are "fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic" (Column 3, lines 57-62) and explains that wherein memory may be external (Column 3, line 49); therefore, any kind of instructions may be used]**. Hinton does not disclose expressly "wherein said reading and writing is performed by way of using an existing translation lookaside buffer (TLB) control processor instruction set" and "wherein said translation lookaside buffer of reduced size is compatible with one or more legacy systems utilizing any existing TLB instructions, software, or commands".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system components.

12. As per **claims 4 and 11**, Hinton discloses "The method of claims 3 and 1" **[See rejection to claims 3 and 1 above]**; however, Hinton does not disclose expressly that "said TLB control processor instruction set comprises a MIPS control processor instruction set."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

13. **Claim 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Bryg et al. (US 6,430,670).

14. As per **claim 7**, Hinton discloses "The method of claim 6" **[See rejection to claim 6 above]** but does not disclose expressly that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Applicant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)]**.

15. **Claims 8-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Riedlinger et al. (US 6,446,187).

16. As per **claims 8-9**, Hinton discloses "The method of claim 6" **[See rejection to claim 6 above]**; however, Hinton does not discloses "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton]**. Applicant has not disclosed that **[having a virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with **[any size of page mask]** because **[it is well known in art that a page mask is used to select a virtual page size (See Riedlinger, Column 4, lines 14-23)]**.

III. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

17. Applicant's arguments filed July 25, 2006 have been fully considered and are partly persuasive.

18. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

IV. ARGUMENTS CONCERNING FORMAL MATTERS

19. The Applicant's traversal of the formal requirements requested by the examiner are addressed in the following section as required by **M.P.E.P. § 707.07(f)**.

Objections to the Claims

20. Objections to the claims are withdrawn.

V. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1st POINT OF ARGUMENT:

21. Regarding Applicant's remark that the argument posed by the Examiner is Section II of the Office Action appears to make an attempt at addressing only Claim 1 of the instant Application, it is the Examiner's position that the same rationale in the rejection of claim 1 is incorporated to the rejection of claims 12, 16 and 18.

2nd POINT OF ARGUMENT:

22. Regarding Applicant's remark that there is no mention in Hinton of a translation lookaside buffer in Figure 1, the Examiner would like to point Applicant's attention to **["TLB 11" Furthermore, Applicant should not "TWB (mini TLB)" in (Figures 2 and 3) which comprises "a small 3-entry instruction mini TLB (62)" (Column 5, line 62-Column 6, line**

5)] and that Hinton does not disclose, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, it is the Examiner's position that Hinton disclosure meets all the limitations required by the claim language as Hinton discloses **["TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14)]**. Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field."

3rd POINT OF ARGUMENT:

23. Regarding Applicant's remark that Hinton does not teach utilizing a bit that corresponds to the least significant bit of a virtual page number as "bit 12" is not a least significant bit as recited in claims 2 and 13, it is the Examiner's position that Hinton discloses this limitation as Applicant's own Specification defines a least significant bit of a virtual page address as bit 12 as it is recited that **["the lest significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)" (Page 3, Paragraph 0026)]**.

4th POINT OF ARGUMENT:

24. Regarding Applicant's remark that Hinton differs from the claimed invention as Hinton describes a translation lookaside buffer (TLB) and a translation write buffer (TWB), it is the Examiner's position that Hinton discloses all of the limitations required by the claim language as **["TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14)]**; therefore, teaching "utilizing a bit from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer," as claimed.

5th POINT OF ARGUMENT:

25. Regarding Applicant's remark challenging the Examiner's official notice that it "would have been obvious to one or ordinary skill in the art at the time of the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system components," it is the Examiner's position that Hinton discloses **[a translation lookaside buffer (TLB) for translating instruction pointers from logical addresses to physical addresses (Column 3, lines 23-25)**

wherein instructions are "fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic" (Column 3, lines 57-62); therefore, any kind of instructions may be used as any instruction used in Hinton's disclosure is an existing/legacy instruction]. Furthermore, it would have been obvious to one of ordinary skill to use any existing instruction set such as a MIPS RX000 RISC control processor instruction set which is well known in the art at the time of the invention as evidenced by **[Kirk (US 5,875,464) (Column 19, lines 42-54)]**.

6th POINT OF ARGUMENT:

26. Regarding Applicant's remark challenging the Examiner's argument that "a recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior art if the prior art has the capacity to do so" may be applied to apparatus claims and not method claims, the Examiner considers this remark persuasive and withdraws the argument that "A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior if prior art has the capability to do so" from the rejection of claims 3, 5, 10, 14 and 20.

7th POINT OF ARGUMENT:

27. Regarding Applicant's remark challenging the Examiner's official noticethat "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type" because one of ordinary skill in the art would have been motivated to select form off the shelf processors at least to reduce cost and take

advantage of existing component design and that Applicants submit that MIPS refers to RISC microprocessor architecture developed by MIPS Technologies (aka MIPS Computer Systems Inc.), the Examiner maintains this rejection as it would have been obvious to one of ordinary skill to use any existing instruction set such as a MIPS RX000 RISC control processor instruction set which is well known in the art at the time of the invention as evidenced by **[Kirk (US 5,875,464) (Column 19, lines 42-54)]**.

8th POINT OF ARGUMENT:

28. Regarding Applicant's remark that a "page mask size ranging from 4 kilobytes to 16 megabytes" is a preferred embodiment (i.e., a preferred range) in which the invention may be realized and that the combination of Hinton and Riedlinger does not disclose this limitation, it is the Examiner's position that the size of a page mask is a matter of design choice as having a mask of a particular size would not have modified the operation of the claimed TLB or the TLB as disclosed by Hinton; therefore, Applicant's invention would have performed equally well with any size of page mask. Furthermore, the Examiner provided the reference to Riedlinger in which **[it is taught that a page mask is used to select a virtual page size (Riedlinger, Column 4, lines 14-23) and the Background section of Applicant's Specification (which describes "prior art") recites "the size of the pages that are accessed by the TLB may range from a few kilobytes to up to several megabytes in size" (Page 1, Paragraph 0005)]**. Therefore, it is the Examiner's position that the since the size of a page of a TLB is variable and a matter of design choice, the page mask used to select a virtual page size may also vary depending on the size of the TLB used and it is also a matter of design choice.

29. All arguments by the Applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated July 25, 2006.

VI. CLOSING COMMENTS

Conclusion

30. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing data of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of the final action.

VII. STATUS OF CLAIMS IN THE APPLICATION

31. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

32. Per the instant office action, **claims 1-20** have received a second action on the merits and are subject of a final rejection.

33. For at least the above reasons it is the examiner's position that the Applicant's claims are not in condition for allowance.

VIII. DIRECTION OF ALL FUTURE REMARKS

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

35. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 5, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
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